WHAT IS CLAIMED IS:

1. A HDD comprising:

at least one write channel including at least one write gate; and

control circuitry controlling the write gate using write control bits to selectively enable writing data bits associated with a servo pattern onto at least one disk.

2. The HDD of Claim 1, wherein the control circuitry writes a servo pattern after the HDD has been sealed.

3. The HDD of Claim 1, wherein the write channel is used during operation to write user data to the disk.

4. The HDD of Claim 1, wherein the control circuitry uses two bits of a ten bit parallel bus as write control bits to indicate whether the write gate should enable writing one or more of the remaining eight bits of the bus to disk.

5. The HDD of Claim 1, wherein the control circuitry uses four bits of an eight bit parallel bus as write control bits to indicate whether the write gate should enable writing one or

more of the remaining four bits of the bus to disk.

6. The HDD of Claim 3, wherein the control circuitry uses a write delay to a next timing mark based on detecting a current timing mark, the time delay including a clock cycle component and a clock phase component, the write channel using the write delay to write the next timing mark and associated portions of the servo pattern to disk.

7. A method for self-writing a servo pattern to a disk using a write channel intended for subsequently writing user data, comprising:

receiving a servo pattern defined by a stream of data bits; and

based on write control bits associated with the servo pattern, enabling and disabling a write gate associated with the write channel without deenergizing the write channel.

8. The method of Claim 7, wherein a write control bit is associated with at least one data bit.

9. The method of Claim 8, wherein a write control bit is associated with one and only one data bit.

10. The method of Claim 8, wherein a write control bit is associated with at least two data bits.

11. The method of Claim 7, comprising writing the servo pattern on the disk after the disk has been sealed in a housing.

12. The method of Claim 7, further comprising:

determining a write delay to a next timing mark based on detecting a current timing mark, the time delay including a clock cycle component and a clock phase component; and

using the write delay to write the next timing mark and associated portions of the servo pattern to disk.

13. A system, comprising:

a hard disk drive controller;

at least one disk onto which the controller writes user data using at least one write channel, the write channel including a write gate; and

means for, at least prior to providing the system to the user, selectively enabling and disabling the write gate while the write channel remains energized to write a servo pattern on the disk.

14. The system of Claim 13, wherein the means for enabling and disabling include write control bits.

15. The system of Claim 14, wherein two write control bits of a ten bit parallel bus establish write control bits to indicate whether the write gate should enable writing one or more of the remaining eight bits of the bus to disk.

16. The system of Claim 14, wherein four bits of an eight bit parallel bus establish write control bits to indicate whether the write gate should enable writing one or more of the remaining four bits of the bus to disk.

17. The system of Claim 13, comprising control circuitry using a write delay to a next timing mark based on detecting a current timing mark, the time delay including a clock cycle component and a clock phase component, the write channel using the write delay to write the next timing mark and associated portions of the servo pattern to disk.

18. A HDD, comprising:

at least one write channel configured for writing user data to a disk; and

control circuitry using the write channel to write at least one timing mark and at

least a portion of a servo pattern using a single write delay determined using a prior timing mark.

19. The HDD of Claim 18, comprising:

at least one write gate in the write channel, the control circuitry controlling the write gate using write control bits to selectively enable writing data bits associated with a servo pattern onto at least one disk.